Third Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define combinational logic. Design a combinational circuit which takes two, 2 bit binary numbers as its input and generates an output equal to 1, when the sum of the two numbers is even. **(10 Marks)**

b. Simplify using Karnaugh map. Write the Boolean equation and realize using NAND gates.
$D = f(w, x, y, z) = \Sigma m (0, 2, 4, 6, 8) + \Sigma d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

OR

2 a. Define canonical SOP and canonical POS. Expand $f = (\bar{a} + b + c)(a + c + \bar{d})$ into canonical POS. **(04 Marks)**

b. Solve using Quine-McCluskey tabulation method,
$f(a, b, c, d) = \Sigma m(0, 1, 4, 5, 9, 10, 12, 14, 15) + \Sigma\phi(2, 8, 13)$
Obtain the minimal form of the given function. Verify the result using k–map. **(12 Marks)**

Module-2

3 a. Define decoder. Implement full subtractor using a decodes. Write the truth table. **(08 Marks)**

b. Compare ripple carry adder and look ahead carry adder. Explain the circuit and operation of a 4 bit binary adder with look ahead carry. **(08 Marks)**

OR

4 a. Design and implement one bit comparator. **(04 Marks)**

b. Implement the multiple functions :
$f_1(a, b, c, d) = \Sigma(0, 4, 8, 10, 14, 15)$ and
$f_2(a, b, c, d) = \Sigma(3, 7, 9, 13)$
using two 3 to 8 decoders, i.e. 74138 ICs. **(06 Marks)**

c. Implement full adder circuit using 8 : 1 multiplexer. **(06 Marks)**

Module-3

5 a. What is gated SR Latch? Explain the operation of gated SR Latch, with a logic diagram, truth table and logic symbol. **(08 Marks)**

b. Derive the characteristic equation of SR, JK, D and T flip-flops with the help of function tables. **(08 Marks)**

OR

6 a. Explain the operation of a switch debouncer built using SR Latch. Draw the supporting waveforms. **(04 Marks)**

b. Explain 0s and 1s catching problem of Master Slave JK flip flop with waveform. Suggest the solution for this problem. **(04 Marks)**

c. What is edge triggered flip flop? With a neat circuit diagram, explain the operation of positive edge triggered D flip flop, using NAND gates. **(08 Marks)**

Module-4

7 a. With the help of neat diagram, explain PISO and PIPO operation of unidirectional shift registers. **(08 Marks)**

b. Design a 4 bit binary ripple 'UP' counter using negative edge triggered JK flip flop. Show the up counter execution with the help of timing diagram. **(08 Marks)**

OR

8 a. Implement a Mod 8 twisted ring counter using D flip flops. Give the counting sequence and decoding gate inputs. **(06 Marks)**

b. Design a synchronous MOD-6 counter using JK flip flop for the following count sequence 0, 2, 3, 6, 5, 1 and repeat. Write the transition table, logic equations and the counter implementation diagram. **(10 Marks)**

Module-5

9 a. Compare Mealy and Moore sequential circuit models with suitable example. **(04 Marks)**

b. For the logic diagram shown in Fig.Q9(b), write the state and output equations. Give the transition table and the state diagram. **(12 Marks)**

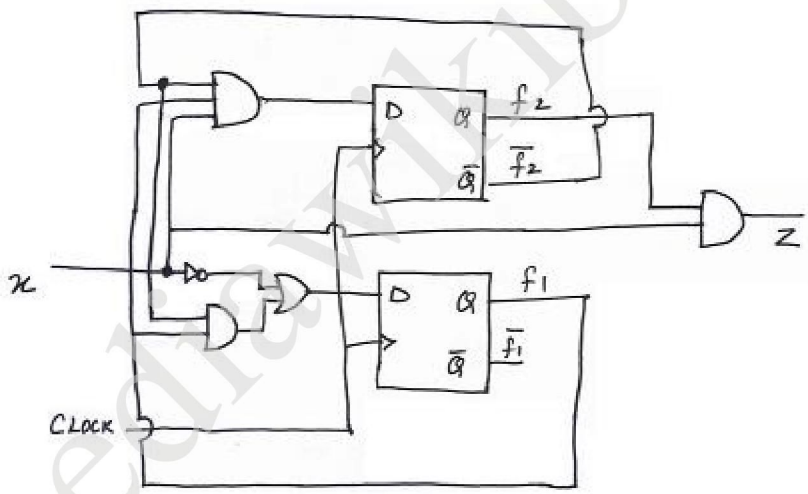

Fig.Q9(b)

OR

10 a. Write the basic recommended steps for the design of a clocked synchronous sequential circuit. **(06 Marks)**

b. How to convert a Mealy machine to a Moore machine? **(02 Marks)**

c. A sequential circuit has one input and one output. The state diagram is shown in Fig.Q10(c). Design a sequential circuit using D flip flop. **(08 Marks)**

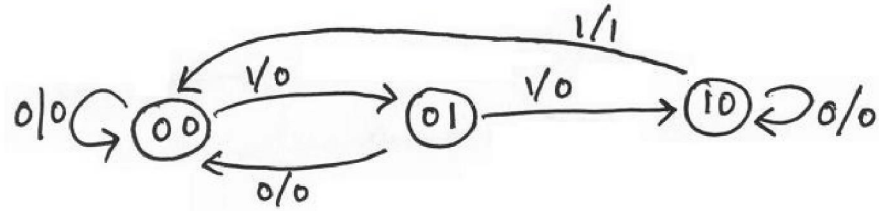

Fig.Q10(c)

17EC34

Third Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Express the following functions into a canonical form:
i) $f_1 = a + bc + bcd$
ii) $f_2 = a(b + c)(b + c + d)$ **(08 Marks)**

b. Represent the number of days in a month for a non-leap year by a truth cable, indicating the output of a invalid inputs if any by '0'. **(06 Marks)**

c. Simplify the given function using K-map method
$f(abcd) = \sum m(1, 2, 4, 11, 13, 14, 15) + d(0, 5, 7, 8, 10)$. **(06 Marks)**

OR

2 a. Find all prime implicants of the function using Quine-industry method and verify the same by K-map method .$f(abcd) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14)$ **(10 Marks)**

b. Find minimal sum and minimal product for the incomplete Boolean function using K-map $f(abcd) = \sum m(6, 7, 9, 10, 13) + d\sum(1, 4, 5, 11, 15)$. **(10 Marks)**

Module-2

3 a. Design two bit magnitude comparator. **(10 Marks)**

b. Design 4:2 priority encoder with a valid output where highest priority is given to the highest bit position. **(10 Marks)**

OR

4 a. Design and realize the Boolean function using IC-74139.
$f_1(ab) = \sum(0, 2)$, $f_2(abc) = \sum(1, 3, 5, 7)$. **(05 Marks)**

b. Explain how look ahead carry adder circuit will reduce the propagation delay with the help of carry propagate and carry generate function. **(08 Marks)**

c. Implement the Boolean function $f(abcd) = \sum(0, 2, 4, 5, 7, 9, 10, 14)$ using multiplexers with two 4:1 MUX with variable 'a' and 'b' are connected to their select lines in first level and one 2:1 MUX with variable 'c' connected to its select line in second level. **(07 Marks)**

Module-3

5 a. With the help of logic circuit and waveforms. Explain switch bouncing applications using SR latch. **(06 Marks)**

b. Write the characteristics equation for SR, JK flip flop. **(06 Marks)**

c. With neat logic diagram, and waveform. Explain the operation of master-slave J-K flip-flop. **(08 Marks)**

OR

6 a. List the difference between combinational and sequentional circuit. **(06 Marks)**

b. Explain the operation of clocked SR flip-flop using NAND-gate. s **(06 Marks)**

c. What is the significance of Edge triggering? Explain the working of positive edge triggered D flip-flop with their function table. **(08 Marks)**

Module-4

7 a. With neat diagram, explain the operation of universal shift register. **(08 Marks)**

b. Design 3 bit binary synchronous down counter using JK Flip Flop. Write excition table, transition table, and logic diagram. **(12 Marks)**

OR

8 a. What is register? With heat circuit diagram, explain the operation of 4-bit ring counter. **(07 Marks)**

b. With logic diagram, sequence table, decoding logic. Explain the operation of mod-7 twisted ring counter. **(07 Marks)**

c. Explain the working of 4 bit binary ripple counter using positive edge triggered T-flip-flop also draw timing diagram, truth table. **(06 Marks)**

Module-5

9 a. Write the difference between Moore and Mealy model with necessary block diagram. **(08 Marks)**

b. Design asynchronous circuit using positive edge triggered J-K flip-flop with minimal combinational gating to generate the following sequence. 0-1-2-0: if input X = 0 and 0 – 2 – 1 – 0; if input X = 1, provide an output which goes high to indicate the non-zero state in the 0-1-2-0 sequence. Is this a mealy machine? **(12 Marks)**

OR

10 a. Design a cyclic mod-8 synchronous binary counter using JK flip-flop. **(10 Marks)**

b. Analyze the given sequential circuit show in Fig.Q.10(b) and obtain.

i) Flip-flop Input and Output Equation
ii) Transition Equation
iii) Transition Table (N)
iv) State Table
v) State Diagram.

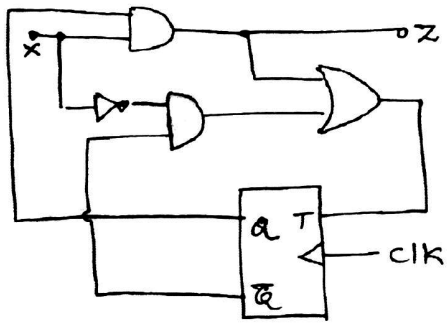

Fig.Q.10(b)

(10 Marks)

CBCS Scheme

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15EC33

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer FIVE full questions, choosing one full question from each module.

Module-1

1 a. Define the following: i) TVUM Table; ii) Combinational circuit; iii) Cannonical SOP; iv) Cannonical POS. **(04 Marks)**

b. Obtain minimal expression using k-map for the following incompletely specified function: $F(a, b, c, d) = \sum_{m}(0,1,4,6,7,9,15) + \sum_{d}(3,5,11,13)$ and draw the circuit diagram using gates. **(06 Marks)**

c. Write the truth table and design a circuit to generate o/p using K-map for the problem statement given: o/p of a combinational circuit having 4 inputs and an o/p, becomes logical '1' when two or more inputs goto logic level '1'. **(06 Marks)**

OR

2 a. Define K-map, incompletely specified function, essential prime implicants and grey code. **(04 Marks)**

b. Obtain minimal logical expression for the given maxterm expression using K-map. $f(a,b,c,d) = \pi_{M}(0,1,4,5,6,7,9,14).\pi_{d}(13,15)$. **(04 Marks)**

c. Use Quine McCluskey's method of minimization to obtain essential prime implicants and minimal expression for the following minterm expression: $f(a, b, c, d) = \sum_{m}(0, 1, 4, 5, 7, 8, 13, 15) + \sum_{d}(2)$. **(08 Marks)**

Module-2

3 a. Define encoder, decoder, priority encoder and multiplexer. **(04 Marks)**

b. Write block diagram representation of a full adder using 3:8 decoders. **(04 Marks)**

c. Design full adder using i) 8:1 MUX and ii) 4:1 MUX. **(08 Marks)**

OR

4 a. Explain Carry look ahead adder with neat diagram and relevant expressions. **(08 Marks)**

b. Design 2-bit comparator and briefly explain. **(08 Marks)**

Module-3

5 a. Define bistable element, latch, flip-flop and function table. **(04 Marks)**

b. Sketch timing diagrams for JK flipflop and D-flip-flop. **(06 Marks)**

c. Explain M/S JK flip-flop with the help of circuit diagram and waveforms. **(06 Marks)**

OR

6 a. Find characteristic equations for T and SR-flip-flops with the help of function tables. **(06 Marks)**

b. Write circuit diagram for the edge triggered D-flip-flop and provide explanation for different input condition. **(06 Marks)**

c. Explain the operation of a switch debouncer built using SR-latch with the help of waveforms. **(04 Marks)**

Module-4

7 a. Define register, asynchronous ripple counter synchronous counter and ring counter. **(04 Marks)**

b. Design mod-8 counter using right shift register. Use D-flip-flop to build register circuit. Explain the operation using function table. **(06 Marks)**

c. Write timing diagrams, counting sequence and the logic diagram for 4-bit ripple counter and briefly explain. **(06 Marks)**

OR

8 a. Explain PIPO and SIPO operations using single diagram. **(06 Marks)**

b. Design Mod-6 synchronous counter using JK flip-flop. The sequence is 000, 001, 011, 100, 101, 111…000. **(07 Marks)**

c. Write state diagram for Mod-5 self correcting counter and briefly explain. The sequence is 000, 001, 101, 110, 111, 000. **(03 Marks)**

Module-5

9 a. What are Melay and Moore models of a sequential circuit? Briefly explain with diagrams. **(04 Marks)**

b. Write characteristic/excitation table for JK flip-flop and explain. **(03 Marks)**

c. Analyze the following sequential circuit. Writ excitation equations K-maps and state diagrams to analyze. **(09 Marks)**

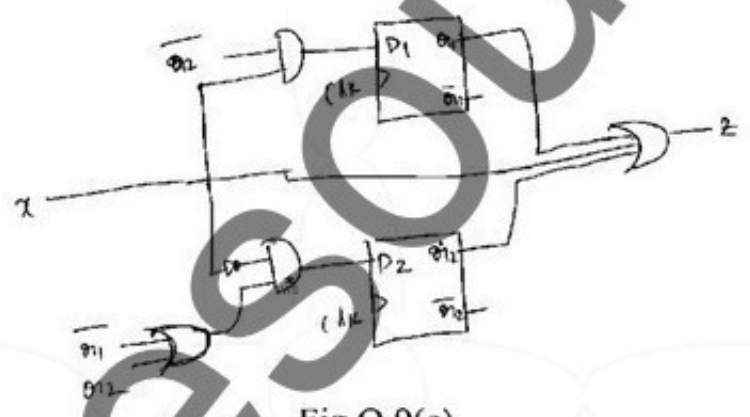

Fig.Q.9(c)

OR

10 a. Write state diagrams for a four state machine using Melay and Moore models and briefly explain. **(04 Marks)**

b. What is a state table? Give an example. **(02 Marks)**

c. Design a counter circuit for the following state table. Follow the standard steps for design. **(10 Marks)**

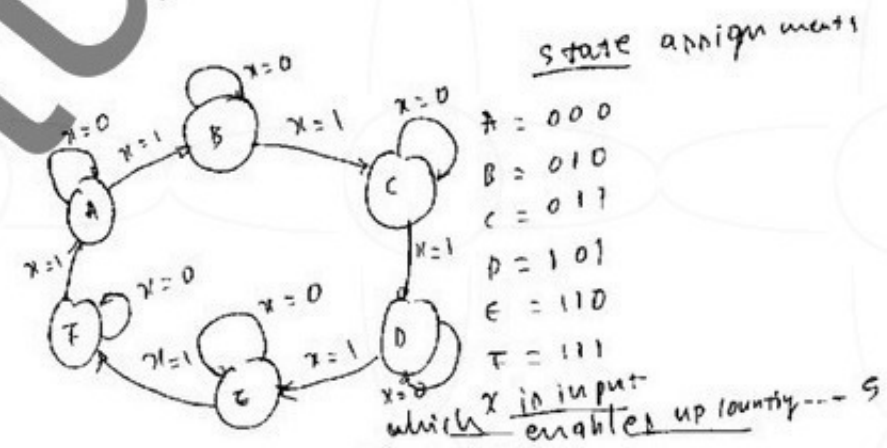

Fig.Q.10(c)

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CBCS Scheme

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Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Identify all prime implicants and essential prime implicants of following function using k – map.
$f(a, b, c, d) = \Sigma m(6, 7, 9, 10, 13) + d.c(1, 4, 5, 11, 15)$
$f(a, b, c, d) = \pi m(1, 2, 3, 4, 9, 10) + d.c(0, 14, 15)$ **(08 Marks)**

b. Find minimal sum for following Boolean function using Quine –McClusky method :
$f(a, b, c, d) = \Sigma m(7, 9, 12, 13, 14, 15) + d.c(4, 11)$. **(08 Marks)**

OR

2 a. Transform each of following canonical expression into other canonical form in decimal notation.
$f(x, y, z) = \Sigma m(0, 1, 3, 4, 6, 7)$
$f((w, x, y, z) = \pi M(0, 1, 2, 3, 4, 6, 12)$. **(04 Marks)**

b. Find a minimal sum for following Boolean function using decimal QM method and PI table reduction.
$f(a, b, c, d) = \Sigma m(1, 3, 6, 8, 9, 10, 12, 14) + d.c(7, 13)$. **(12 Marks)**

Module-2

3 a. Implement following functions using single 3 : 8 decoder
$f_1(a, b, c) = \pi M(2, 3, 4, 5, 7)$
$f_2(a, b, c) = \Sigma m(1, 3, 5)$. **(04 Marks)**

b. What is magnitude comparator? Design a two bit digital comparator by writing TT, relevant expression and logic diagram. **(12 Marks)**

OR

4 a. Implement $f(a, b, c, d) = \Sigma m(0, 1, 5, 6, 7, 10, 15)$ using
i) 8 : 1 MUX with a, b, c as select lines
ii) 4 : 1 MUX with a, b as select lines. **(08 Marks)**

b. What are the problems associated with basic encoder? Explain how can these problems be overcome by priority encoder considering 8 input lines. **(08 Marks)**

Module-3

5 a. What is flip-flop. Discuss working principle of SR flip-flop with its TT. Also highlight role of SR f/f in switch debouncer circuit. **(08 Marks)**

b. What is significance of edge triggering? Explain working of +ve edge triggered D flip-flop with their functional table. **(08 Marks)**

OR

6 a. Explain the working of M/S JK flip-flop with functional table and timing diagram. Show how race condition is overcome. **(10 Marks)**

b. Obtain characteristic equation for following flip –flops. i) JK ii) SR. **(06 Marks)**

Module-4

7 a. Realize a 3 bit binary synchronous up counter using JK flip-flop. Write excitation table, transition table and logic diagram. **(10 Marks)**

b. Explain SIPO and PISO shift registers with relevant logic diagrams. **(06 Marks)**

OR

8 a. Explain the working principle of 4bit binary ripple counter configured using +ve edge triggered T – F/F. Also draw timing diagram. **(08 Marks)**

b. Explain the operation of universal shift register with a neat diagram. **(08 Marks)**

Module-5

9 a. Distinguish between Moore and Mealy model with necessary block diagram. **(06 Marks)**

b. Construct mealy state diagram that will detect input sequence 10110, when input pattern is detected, z is asserted high. Give state diagram for each state. **(10 Marks)**

OR

10 a. Design a cyclic mod 8 synchronous binary counter using JK flip-flop. Give state diagram, transition table and excitation table. **(08 Marks)**

b. Analyse the following sequential circuit shown in figure and obtain :

i) Flip-flop input and output equation
ii) Transition equation (ch.equ)
iii) Transition table
iv) State table
v) Draw state diagram. **(08 Marks)**

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CBCS SCHEME

USN | | | | | | | | | | |

17EC34

Third Semester B.E. Degree Examination, Dec.2018/Jan.2019

Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Convert $x = \bar{a}b + bc$ to canonical SOP form. **(02 Marks)**

b. Simplify $G = f(w,x,y,z) = \pi M(1,3,8,10,12,13,14,15)$ in POS form and implement using NOR gates. **(08 Marks)**

c. Simplify the following using Quine-McClusky's minimization technique.
$V = f(a, b, c, d) = \sum m(1, 3, 4, 5, 6, 9, 11, 12, 13, 14)$ **(10 Marks)**

OR

2 a. Convert $P = (\overline{w} + x)(y + \overline{z})$ to canonical POS form. **(03 Marks)**

b. Simplify $P = f(a, b, c, d) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$ in SOP form and implement using NAND gates. **(07 Marks)**

c. Simplify using Quine-McClusky's minimization technique.
$V = f(a, b, c, d) = \sum m(1, 5, 7, 9, 13, 15) + \sum d(8, 10, 11, 14)$ **(10 Marks)**

Module-2

3 a. Implement $f_1(a, b, c) = \sum m(1, 3, 5)$, $f_2(a, b, c) = \sum m(0, 1, 6)$ using 74138, 3:8 decoder. **(06 Marks)**

b. With a neat circuit diagram explain the carry look ahead adder with relevant expressions. **(10 Marks)**

c. Design a one-bit comparator, implement using suitable gates. **(04 Marks)**

OR

4 a. Using 74151, 8:1 Mux, realize the Boolean function $F(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 10, 15)$ with b, c, d as select lines. **(04 Marks)**

b. With neat circuit diagram, explain the keypad interface using 74147, 10 line to BCD encoder. **(10 Marks)**

c. Design a full subtractor and implement using logic gates. **(06 Marks)**

Module-3

5 a. Discuss the working principle of Gated SR latch with its truth Table. **(06 Marks)**

b. Explain the operation of Switch debouncer built using SR latch with the help of circuit and waveforms. **(08 Marks)**

c. Obtain the characteristic equations of JK flip flop and SR flip flop. **(06 Marks)**

OR

6 a. What is race around condition? How it can be overcome? **(02 Marks)**

b. Explain the working of MS-JK flip flop with logic symbol and timing diagram. **(10 Marks)**

c. Explain the working of +ve edge triggered D flip flop with the functional table. **(08 Marks)**

Module-4

7 a. Explain the working of four bit ripple counter using +ve edge triggered T flip-flops with the counting sequence table and timing diagram. **(10 Marks)**

b. Explain the SIPO and SISO operation of shift register with relevant logic diagram and the truth table. **(06 Marks)**

c. Explain the operation of ring counter using logic diagram and truth table. **(04 Marks)**

OR

8 a. Explain Universal Shift Register with the help of logic diagram and mode control table. **(10 Marks)**

b. Realize a three-bit binary synchronous up counter using JK flip flops. **(10 Marks)**

Module-5

9 a. Construct a Mealy state diagram that will detect input sequence 10110, when input pattern is detected Z is asserted high. Write the state diagram. **(10 Marks)**

b. Design a synchronous counter using T flip flops to count the sequence 0, 2, 3, 6, 5, 1, 0, 2, ... Write the excitation table and state diagram and logic diagram. **(10 Marks)**

OR

10 a. Explain Mealy and Moore model of clocked synchronous sequential circuit with the block diagram. **(08 Marks)**

b. For the logic diagram given in Fig.Q10(b):
i) Derive the excitation and output equations
ii) Write the state equations
iii) Construct transition table and state table
iv) Draw the state diagram

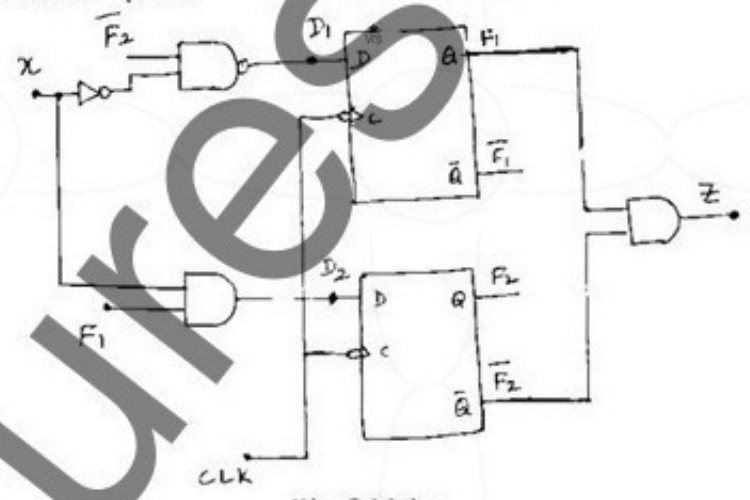

Fig.Q10(b) **(12 Marks)**

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Third Semester B.E. Degree Examination, June/July 2019
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Write the switching equation for a digital circuit with four inputs and whose output is '1' if majority of its inputs are '1'. **(04 Marks)**

b. Place the following equations into proper canonical forms and write its decimal notations also :

i) $P = f(a,b,c) = a\bar{b} + a\bar{c} + bc$

ii) $Q = f(x,y,z) = (x + \bar{y})(\bar{y} + z)$. **(06 Marks)**

c. Solve using k – map and implement using only NAND gates

$B = f(w,x,y,z) = \Sigma(1,2,3,4,9) + \Sigma d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

OR

2 a. Solve using K Map

$A = f(w, x, y, z) = \pi (1, 2, 3, 4, 8, 9, 10, 11, 12, 13, 14, 15)$

and implement using NOR gates only. **(06 Marks)**

b. Simplify using Quine Mc Clusky method :

$D = f(a, b, c, d) = \Sigma(0, 1, 2, 3, 6, 7, 8, 9 14, 15)$

Show the prime implicant table to determine the EPIs. **(10 Marks)**

Module-2

3 a. Design a combinational circuit that multiplies two 2bit binary values, and produces 4-bit product. Get the minterms for P_0, P_1, P_2 and P_3. Simplify only for P_2. **(08 Marks)**

b. Design a 4 to 16 decoder using 3 to 8 decoders (74LS138) only and realize the function :

$P = f(w, x, y, z) = \Sigma(1, 4, 8, 13)$

$Q = f(w, x, y, z) = \Sigma(2, 7, 13, 14)$. **(08 Marks)**

OR

4 a. Design a 2 bit magnitude comparator and get an expression for A < B only, which is the minimal expression. **(08 Marks)**

b. Explain a carry look ahead adder with a neat diagram and relevant expressions. **(08 Marks)**

Module-3

5 a. Explain an SR latch using NOR gates with circuit diagram function table and timing diagram. **(06 Marks)**

b. Explain a positive edge triggered D flip flop with circuit diagram, function table and timing diagram. **(10 Marks)**

OR

6 a. What is race around? How is it overcome in master slave JK F/F. Explain MS JK with relevant circuit diagram, function table. **(10 Marks)**

b. Derive the characteristics equation for :
i) SR F/F ii) JK F/F iii) D F/F iv) T F/F. **(06 Marks)**

Module-4

7 a. Given an universal shift register, sketch its diagram only for left shift operates and explain its working. **(08 Marks)**

b. What is a twisted ring counter? Sketch its diagram and explain its counting sequence and also give the bits that determine a state uniquely. **(08 Marks)**

OR

8 a. Design a model synchronous counter for the sequence, using a D flip-flop [Refer Fig.Q8(a)].

Fig.Q8(a) **(08 Marks)**

b. Explain with net diagram, the counting sequence and timing diagram, the working of a 4 bit binary ripple counter, using positive edge triggered T flip flop. **(08 Marks)**

Module-5

9 a. Draw and explain the Mealy and Moore sequential circuit models. **(06 Marks)**

b. Analyze the following sequential circuit and draw its state diagram.[Refer Fig.Q9(b)]. **(10 Marks)**

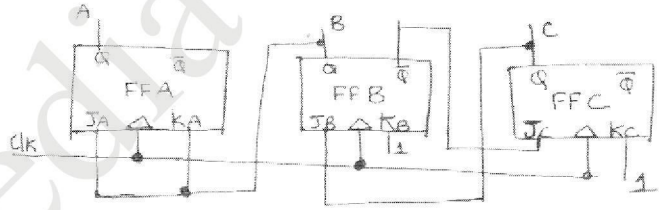

Fig.Q9(b)

OR

10 a. Represent a Moore circuit notation of a JK flip-flop through state diagram and explain. **(06 Marks)**

b. Design a modulo 8 synchronous counter with :
i) state diagram ii) state table iii) transition table iv) excitation table, kmap and logic diagram **(10 Marks)**

Third Semester B.E. Degree Examination, June/July 2019
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Construct a truth table and write a Boolean expression for the problem statement. An output variable Y is to be true when the value of inputs exceeds 4. The weights for each input variable is a = 4, b = 3, c = –1, and d = 1. Design the logic circuit for the obtained expression. **(10 Marks)**

b. Place the equation $P = f(a, b, c) = ab + \bar{a}c + b\bar{c}$ into proper canonical form and write the minterms. **(05 Marks)**

c. What do you mean by canonical SOP and canonical POS? Explain with example? **(05 Marks)**

OR

2 a. Simplify K = f(w, x, y, z) = Σm(0, 1, 5, 13, 15) + Σd(2, 7, 10, 14) using K-map method. Draw the logic diagram for obtained expression. **(10 Marks)**

b. Simplify D = f(a, b, c, d) = Σm(0, 1, 2, 3, 6, 7, 8, 9, 12, 15) using QM – method, verify the same using K–map. Draw the logic diagram for simplified expression. **(10 Marks)**

Module-2

3 a. What is an encoder? Design 4 to 2 priority encoder? **(08 Marks)**

b. Realize the function X = f(a, b, c, d) = Σm(0, 3, 7, 10, 13) using 74LS138 ICs. **(08 Marks)**

c. Design 4 : 1 Mux and draw the logic diagram using basic gates. **(04 Marks)**

OR

4 a. Implement f(a, b, c, d) = Σm(0, 1, 5, 6, 7, 10, 15) using 8 : 1 Mux with a, b, c as select lines. **(08 Marks)**

b. Design a binary full subtractor using NAND gates only. **(06 Marks)**

c. Explain about carry look ahead adder. **(06 Marks)**

Module-3

5 a. Obtain the characteristic equations for D and T flip-flops. **(08 Marks)**

b. Explain the operation of SR–Flip-Flop with the help of logic diagram. Draw functional table. **(08 Marks)**

c. What is race around condition? Explain with diagram. **(04 Marks)**

OR

6 a. Explain the working of master slave J-K flip flop with the help of logic diagram. Draw the timing diagrams of the same. **(10 Marks)**

b. Explain D-flip-flop operation using positive edge triggered clock. **(06 Marks)**

c. Write two-two difference between :

i) Combinational and sequential logic

ii) Latch and flip-flop. **(04 Marks)**

Module-4

7 a. What is register? Explain with diagram of 4-bit serial-in parallel-out shift register. **(10 Marks)**

b. Explain 3-bit asynchronous up and down binary counters. **(10 Marks)**

OR

8 a. Design mod-5 ripple counter using T-flip-flops. **(08 Marks)**

b. Design 3-bit synchronous up counter. **(08 Marks)**

c. Compare asynchronous and synchronous counters. **(04 Marks)**

Module-5

9 a. Design a Mealy type sequence detector to detect a serial input sequence of 101. **(10 Marks)**

b. Design 2-bit synchronous up counter. **(10 Marks)**

OR

10 a. Analyze the following sequential circuit, by writing input and output equations, state table and state diagram. **(12 Marks**

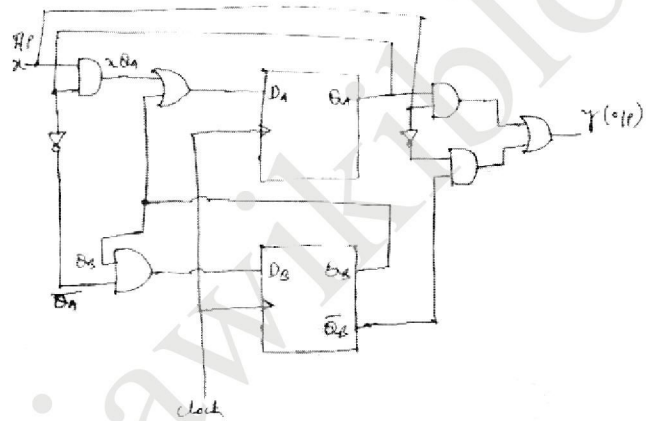

Fig.Q10(a)

b. What are Mealy and Moore models? Explain briefly with diagram. **(04 Marks)**

c. Draw a sate table and state diagram with an example. **(04 Marks)**

CBCS Scheme

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15EC33

Third Semester B.E. Degree Examination, June/July 2017
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Convert the given Boolean function into
   i) $Y = f(a, b, c) = (a + b)(a + c)$ minterm canonical form **(04 Marks)**
   ii) $P = f(a, b, c) = (a + b)(b + c)(\overline{c} + a)$ maxterm canonical form. **(04 Marks)**

b. Using K-map determine the minimal sum of product expression and realize the simplified expression using only NAND gates.
$M = f(W, X, Y, Z) = \sum (1, 4, 5, 6, 11, 12, 13, 14, 15)$. **(08 Marks)**

OR

2 a. Simplify the given Boolean function using Quine – McCluskey method :
$Y = f(a, b, c, d) = \sum (0, 2, 3, 5, 8, 10, 11)$. Verify the result using k-map. **(12 Marks)**

b. Distinguish between prime implicant and Essential prime implicant. **(04 Marks)**

Module-2

3 a. Define Decoder. Implement the following multiple output function using IC 74138 and external gates. Also write the truth table.
$P = f_1(X, Y, Z) = \sum (1, 2, 5, 6)$
$Q = f_2(X, Y, Z) = \pi (3, 5, 6, 7)$. **(06 Marks)**

b. Implement the following Boolean function using 8:1 multiplexer :
$Y = f(A, B, C, D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$ **(10 Marks)**

OR

4 a. Design and implement 4-bit look ahead carry adder. **(08 Marks)**

b. Design and implement BCD to Excess-3 code converter. **(08 Marks)**

Module-3

5 a. Explain the working principle of gated SR latch. **(06 Marks)**

b. Explain the working of master slave JK flip-flop with the help of a logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

OR

6 a. With a neat logic diagram, explain the working of positive edge triggered D flip-flop. Also draw the timing diagram. **(08 Marks)**

b. Derive the characteristic equation for JK and T flip-flop. **(08 Marks)**

Module-4

7 a. Describe the working principle of universal shift register with the help of logic diagram and mode control table. **(08 Marks)**

b. Illustrate the operation of 4-bit binary ripple counter using logic diagram and timing diagram. **(08 Marks)**

OR

8 a. Design a synchronous Mod-6 counter using clocked T flip-flop. **(10 Marks)**
b. Explain Mod-4 ring counter using D flip-flop. **(06 Marks)**

Module-5

9 a. Explain Mealy and Moore sequential circuit models. **(04 Marks)**
b. For the logic diagram shown in Fig Q 9(b).
i) Write input and output equations
ii) Construct transition table
iii) Draw state diagram. **(12 Marks)**

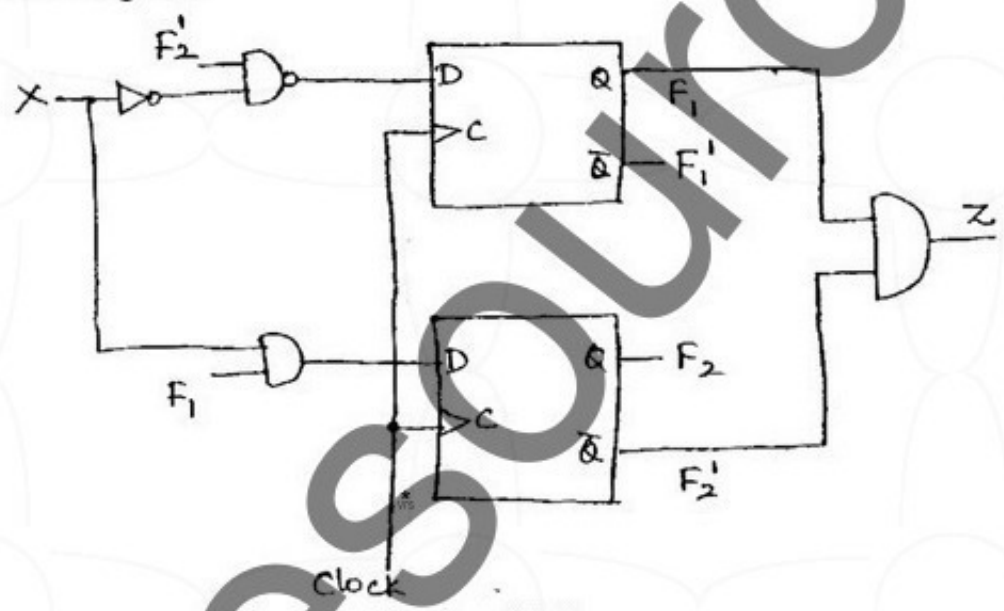

Fig Q9(b)

OR

10 a. Define the terms as applied to sequential circuit :
Input variable, output variable, Excitation variable and state variable. **(04 Marks)**
b. Design a sequential circuit for a state diagram shown in Fig Q 10(b). **(12 Marks)**

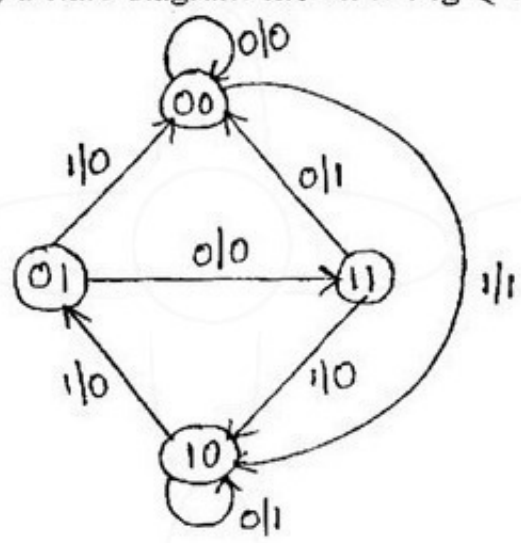

Fig Q10(b)

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CBCS Scheme

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15EC33

Third Semester B.E. Degree Examination, June/July 2018
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Given, F = A(B + C) + D, obtain : i) minimal SOP ii) minimal POS iii) canonical SOP iv) canonical POS. **(08 Marks)**

b. Realize a circuit for Ex-NOR using only four NOR gates. **(02 Marks)**

c. Simplify the function using K-map. :
$Y = f(a,b,c,d) = \sum_m (0,1,2,3,5,6,8,10,15)$.
Write the simplified SOP expression. **(06 Marks)**

OR

2 a. Simplify the following function using Quine – McClusky method :
$P = f(a, b, c, d) = \Sigma_m(0, 2, 3, 5, 8, 10, 11, 13)$. **(06 Marks)**

b. Reduce the following Boolean function using K-map and realize the simplified expression using NOR gates.
$T = f(a, b, c, d) = \Sigma_m(0, 2, 3, 5, 6, 7, 8, 9) + \Sigma_d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

c. Prove that, $ABC + AB\overline{C} + A\overline{B}C + \overline{A}BC = AB + BC + CA$ **(04 Marks)**

Module-2

3 a. Design a binary full subtractor using logic gates. Write a truth table Implement the logic circuit using basic gates. **(06 Marks)**

b. Define magnitude comparator. Design a two bit binary comparator and implement with suitable logic gates. **(10 Marks)**

OR

4 a. Implement full adder using 4 : 1 multiplexer (MUX). **(08 Marks)**

b. With a neat logic diagram, explain carry look ahead adder. **(08 Marks)**

Module-3

5 a. Obtain the characteristic equation for D and T flip-flop. **(04 Marks)**

b. Explain the working of a master–slave SR flip-flop with the help of a logic diagram, function table, logic symbol and timing diagram. **(08 Marks)**

c. Differentiate sequential logic circuit and combinational logic circuit. **(04 Marks)**

OR

6 a. Explain the working of master slave JK flip-flops with functional table and timing diagram. Show how race around condition is over come. **(08 Marks)**

b. Discuss the difference between a flip-flop and latch. **(04 Marks)**

c. Derive the characteristic equations of SR and JK flip-flops. **(04 Marks)**

Module-4

7 a. Design a synchronous mod-5 counter using JK flip-flops and implement it. **(08 Marks)**

b. Design synchronous mod-6 counter using D flip-flop to generate the count sequence, (0, 2, 3, 6, 5, 1, 0). **(08 Marks)**

OR

8 a. Design divide by 6 synchronous counter using T – flip-flops. Write state table and reduce the expression using K-map. **(06 Marks)**

b. Compare synchronous and asynchronous counters. **(04 Marks)**

c. Design mod-6 ripple counter using T flip-flops. **(06 Marks)**

Module-5

9 a. Design a Moore type sequence detector to detect a serial input sequence of 101. **(08 Marks)**

b. Design a synchronous counter using JK – flip-flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2. Use state diagram and state table. **(08 Marks)**

OR

10 a. Explain the Mealy model and Moore model of a clocked synchronous sequential network. **(08 Marks)**

b. Design a Mealy type sequence detector to detect a serial input sequence of 101. **(08 Marks)**

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CBCS SCHEME

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15EC33

Third Semester B.E. Degree Examination, June/July 2019
Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Write the switching equation for a digital circuit with four inputs and whose output is '1' if majority of its inputs are '1'. **(04 Marks)**

b. Place the following equations into proper canonical forms and write its decimal notations also :

i) $P = f(a,b,c) = a\bar{b} + a\bar{c} + bc$

ii) $Q = f(x,y,z) = (x + \bar{y})(\bar{y} + z)$. **(06 Marks)**

c. Solve using k – map and implement using only NAND gates

$B = f(w,x,y,z) = \Sigma(1,2,3,4,9) + \Sigma d(10, 11, 12, 13, 14, 15)$. **(06 Marks)**

OR

2 a. Solve using K Map

$A = f(w, x, y, z) = \pi (1, 2, 3, 4, 8, 9, 10, 11, 12, 13, 14, 15)$

and implement using NOR gates only. **(06 Marks)**

b. Simplify using Quine Mc Clusky method :

$D = f(a, b, c, d) = \Sigma(0, 1, 2, 3, 6, 7, 8, 9 14, 15)$

Show the prime implicant table to determine the EPIs. **(10 Marks)**

Module-2

3 a. Design a combinational circuit that multiplies two 2bit binary values, and produces 4-bit product. Get the minterms for P_0, P_1, P_2 and P_3. Simplify only for P_2. **(08 Marks)**

b. Design a 4 to 16 decoder using 3 to 8 decoders (74LS138) only and realize the function :

$P = f(w, x, y, z) = \Sigma(1, 4, 8, 13)$

$Q = f(w, x, y, z) = \Sigma(2, 7, 13, 14)$. **(08 Marks)**

OR

4 a. Design a 2 bit magnitude comparator and get an expression for A < B only, which is the minimal expression. **(08 Marks)**

b. Explain a carry look ahead adder with a neat diagram and relevant expressions. **(08 Marks)**

Module-3

5 a. Explain an SR latch using NOR gates with circuit diagram function table and timing diagram. **(06 Marks)**

b. Explain a positive edge triggered D flip flop with circuit diagram, function table and timing diagram. **(10 Marks)**

OR

6 a. What is race around? How is it overcome in master slave JK F/F. Explain MS JK with relevant circuit diagram, function table. **(10 Marks)**

b. Derive the characteristics equation for :
i) SR F/F ii) JK F/F iii) D F/F iv) T F/F. **(06 Marks)**

Module-4

7 a. Given an universal shift register, sketch its diagram only for left shift operates and explain its working. **(08 Marks)**

b. What is a twisted ring counter? Sketch its diagram and explain its counting sequence and also give the bits that determine a state uniquely. **(08 Marks)**

OR

8 a. Design a model synchronous counter for the sequence, using a D flip-flop [Refer Fig.Q8(a)].

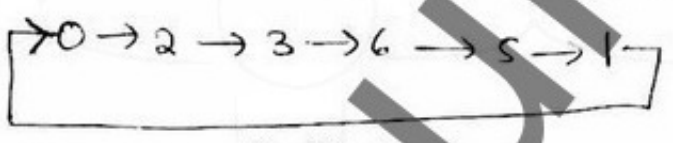

Fig.Q8(a) **(08 Marks)**

b. Explain with net diagram, the counting sequence and timing diagram, the working of a 4 bit binary ripple counter, using positive edge triggered T flip flop. **(08 Marks)**

Module-5

9 a. Draw and explain the Mealy and Moore sequential circuit models **(06 Marks)**

b. Analyze the following sequential circuit and draw its state diagram.[Refer Fig.Q9(b)]. **(10 Marks)**

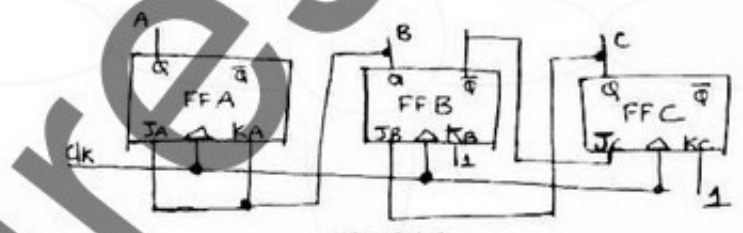

Fig.Q9(b)

OR

10 a. Represent a Moore circuit notation of a JK flip-flop through state diagram and explain. **(06 Marks)**

b. Design a modulo 8 synchronous counter with :
i) state diagram ii) state table iii) transition table iv) excitation table, kmap and logic diagram **(10 Marks)**

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